Fig. 1

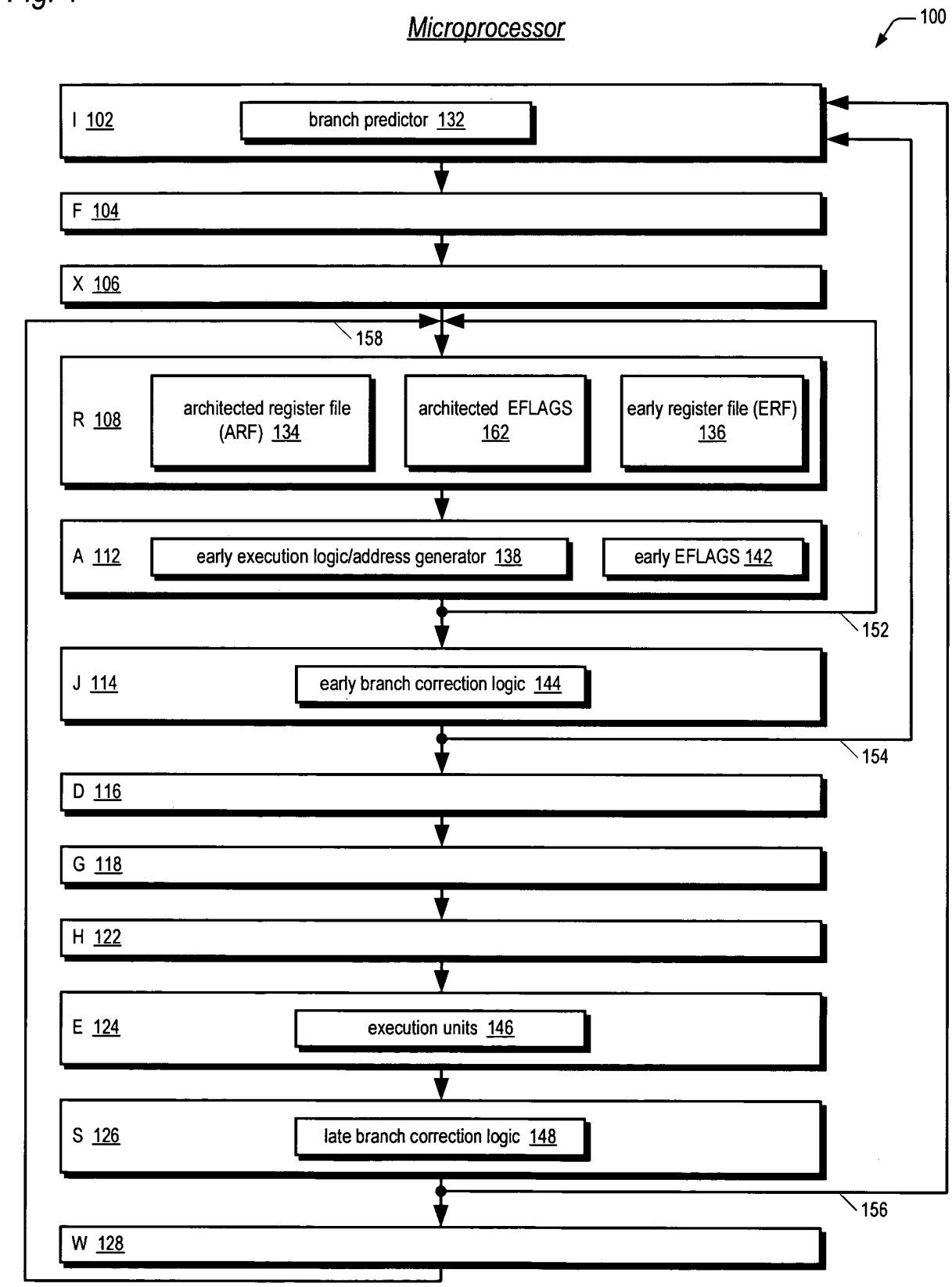

Microprocessor
100
I 102
branch predictor 132
F 104
X 106
158
R 108
architected register file (ARF) 134
architected EFLAGS 162
early register file (ERF) 136
A 112
early execution logic/address generator 138
early EFLAGS 142
152
J 114
early branch correction logic 144
154
D 116
G 118
H 122
E 124
execution units 146
S 126
late branch correction logic 148
156
W 128

Fig. 2

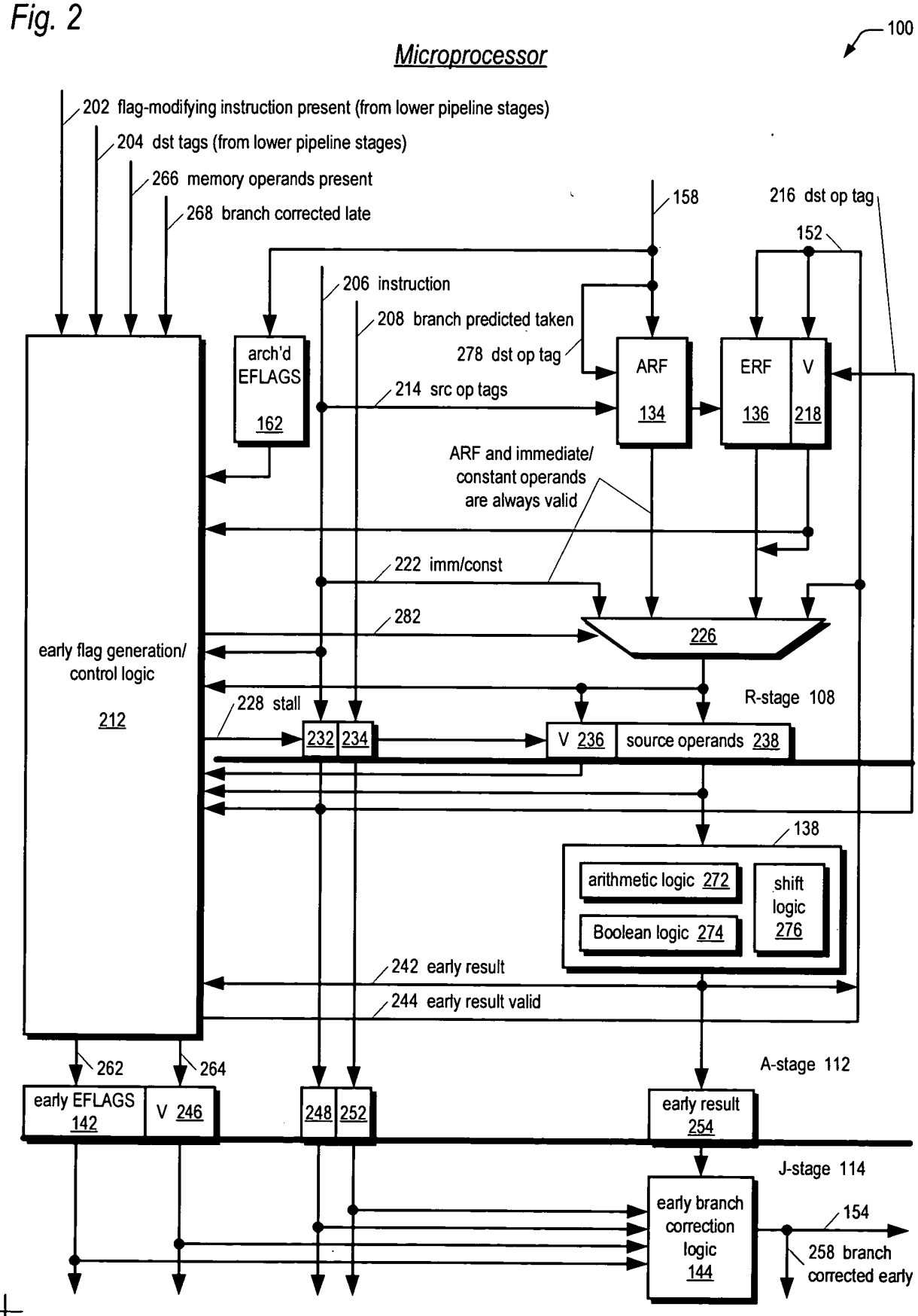

100
Microprocessor
202 flag-modifying instruction present (from lower pipeline stages)
204 dst tags (from lower pipeline stages)
266 memory operands present
268 branch corrected late
158
216 dst op tag
152
206 instruction
208 branch predicted taken
278 dst op tag
arch'd EFLAGS 162
214 src op tags
ARF 134
ERF 136
V 218
ARF and immediate/ constant operands are always valid
222 imm/const
282
226
early flag generation/ control logic 212
228 stall
R-stage 108
232 234
V 236
source operands 238
138
arithmetic logic 272
shift logic 276
Boolean logic 274
242 early result
244 early result valid
262
264
A-stage 112
early EFLAGS 142
V 246
248 252
early result 254
J-stage 114
early branch correction logic 144
154
258 branch corrected early

Fig. 3

Architected Register File, Early Register File,
Architected EFLAGS, Early EFLAGS

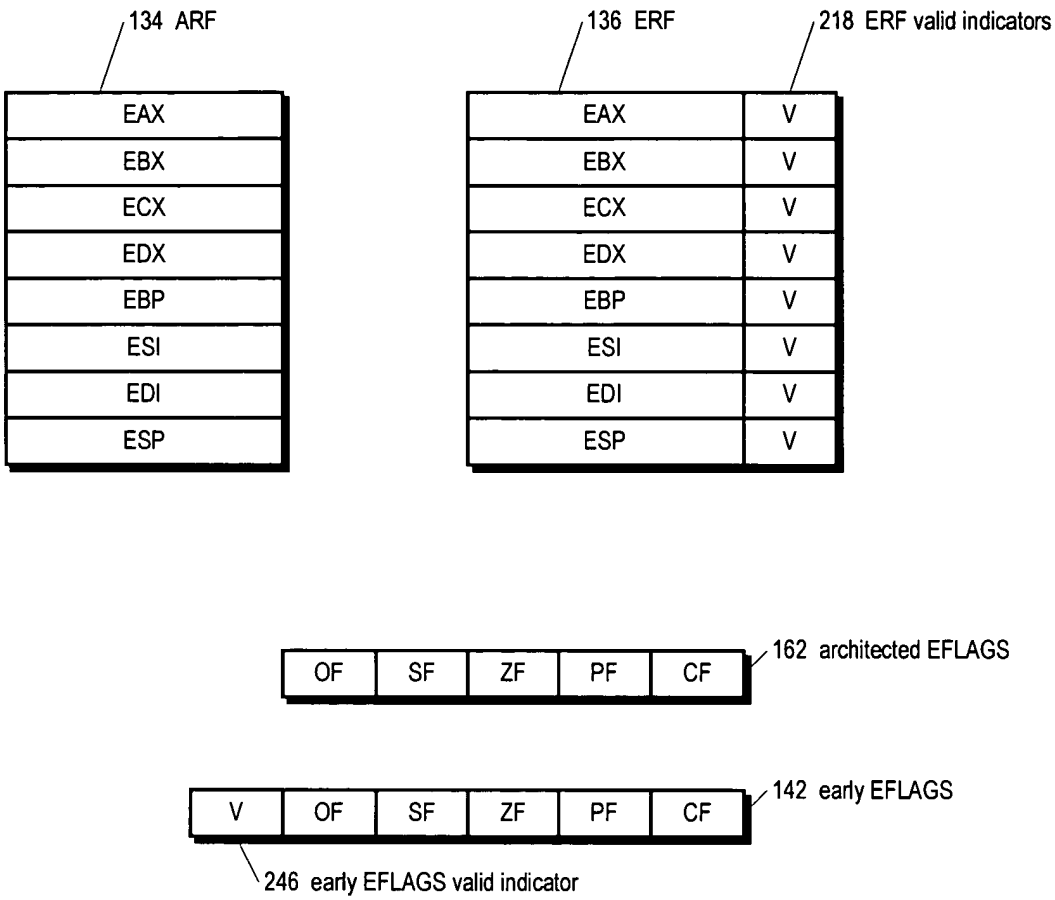


Fig. 4A

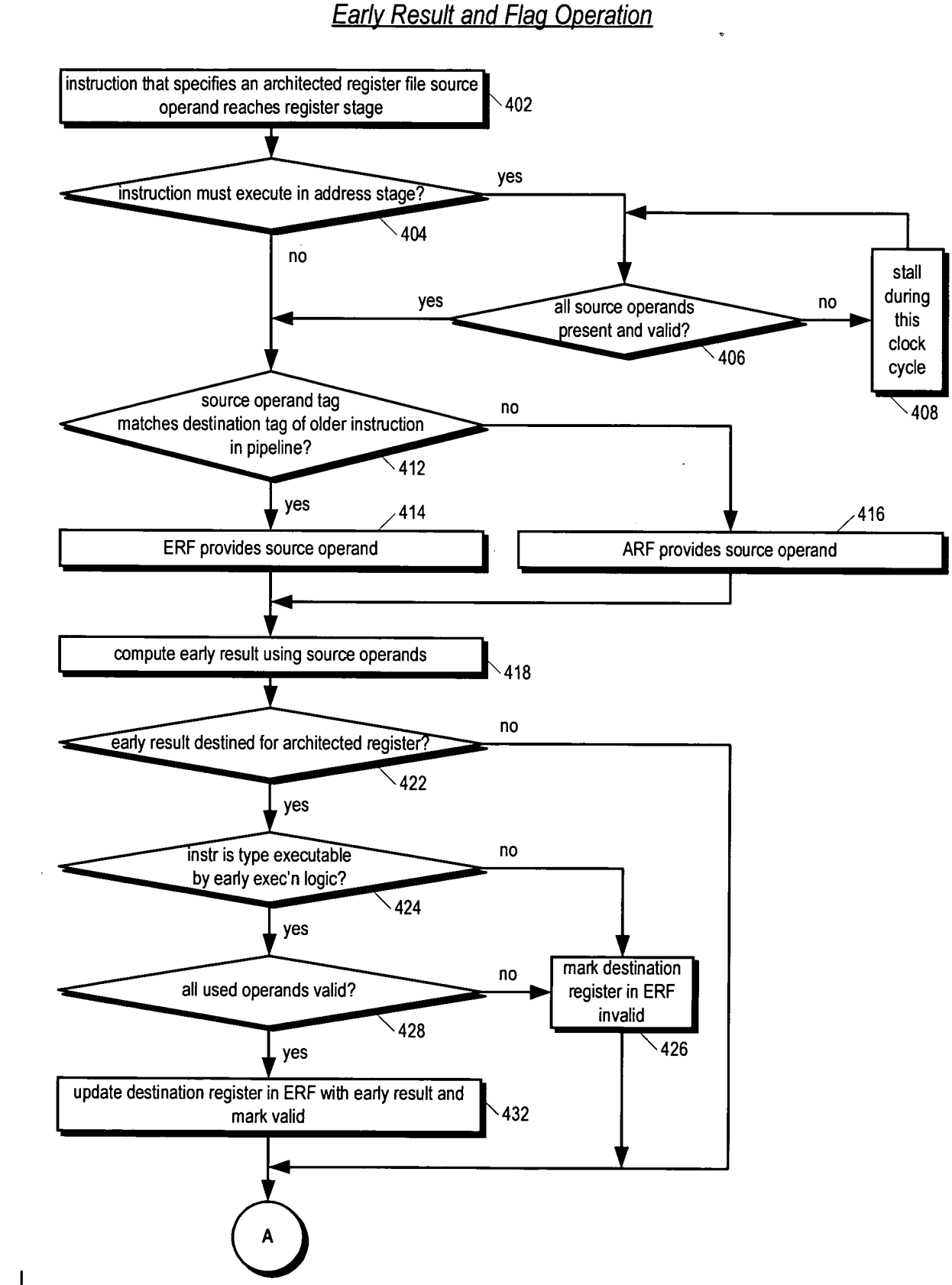

Early Result and Flag Operation
instruction that specifies an architected register file source operand reaches register stage
402
instruction must execute in address stage?
404
yes
no
all source operands present and valid?
406
yes
no
stall during this clock cycle
408
source operand tag matches destination tag of older instruction in pipeline?
412
no
yes
414
ERF provides source operand
416
ARF provides source operand
compute early result using source operands
418
early result destined for architected register?
422
no
yes
instr is type executable by early exec'n logic?
424
no
yes
all used operands valid?
428
no
yes
mark destination register in ERF invalid
426
update destination register in ERF with early result and mark valid
432
A

Fig. 4B

Early Result and Flag Operation (cont'd)

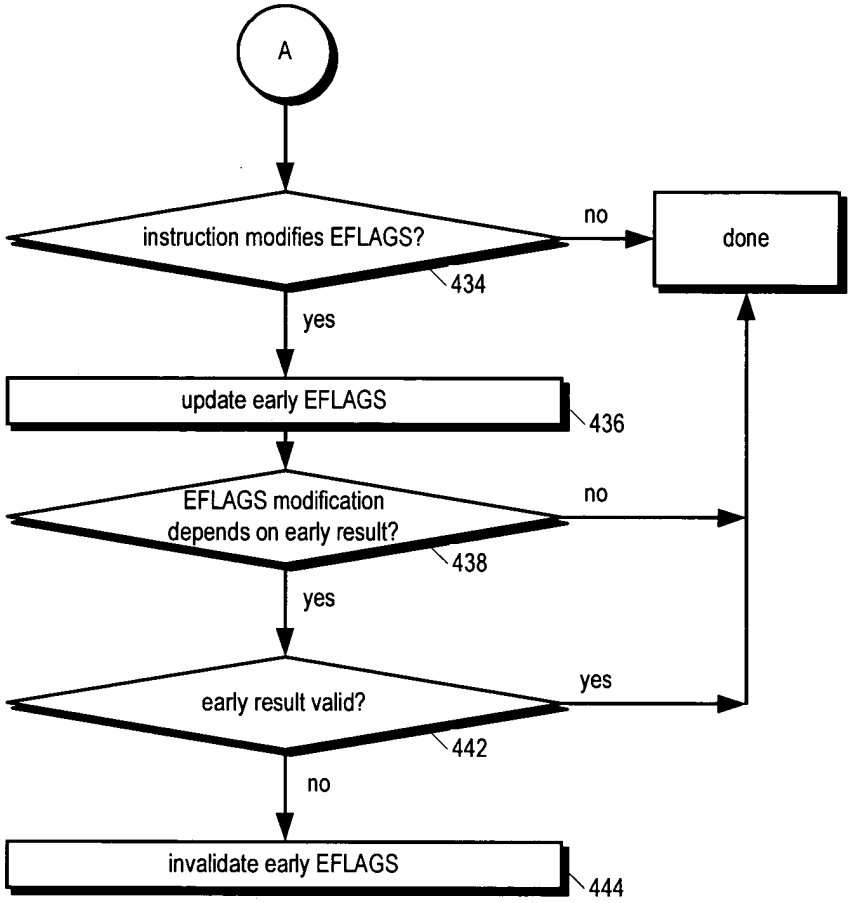


Fig. 5

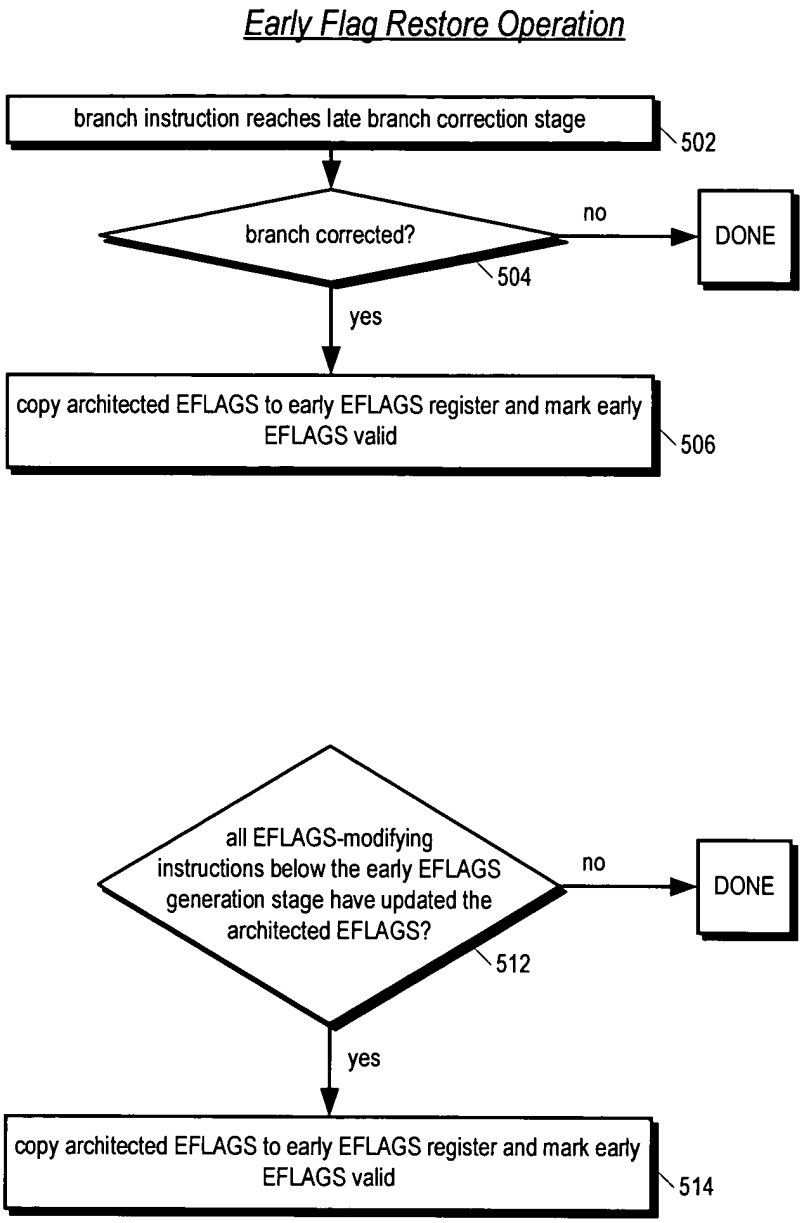

Early Flag Restore Operation
branch instruction reaches late branch correction stage
502
branch corrected?
504
no
DONE
yes
copy architected EFLAGS to early EFLAGS register and mark early EFLAGS valid
506
all EFLAGS-modifying instructions below the early EFLAGS generation stage have updated the architected EFLAGS?
512
no
DONE
yes
copy architected EFLAGS to early EFLAGS register and mark early EFLAGS valid
514

Fig. 6

Early Branch Correction

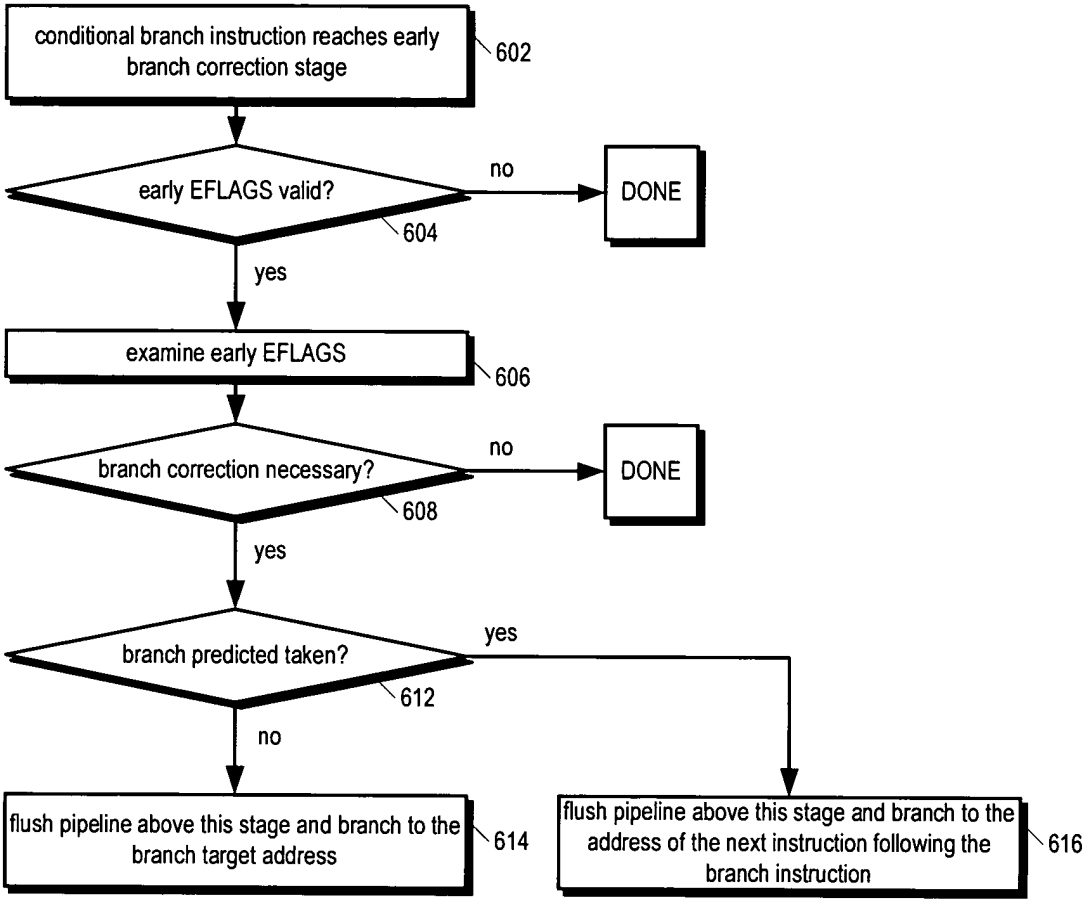
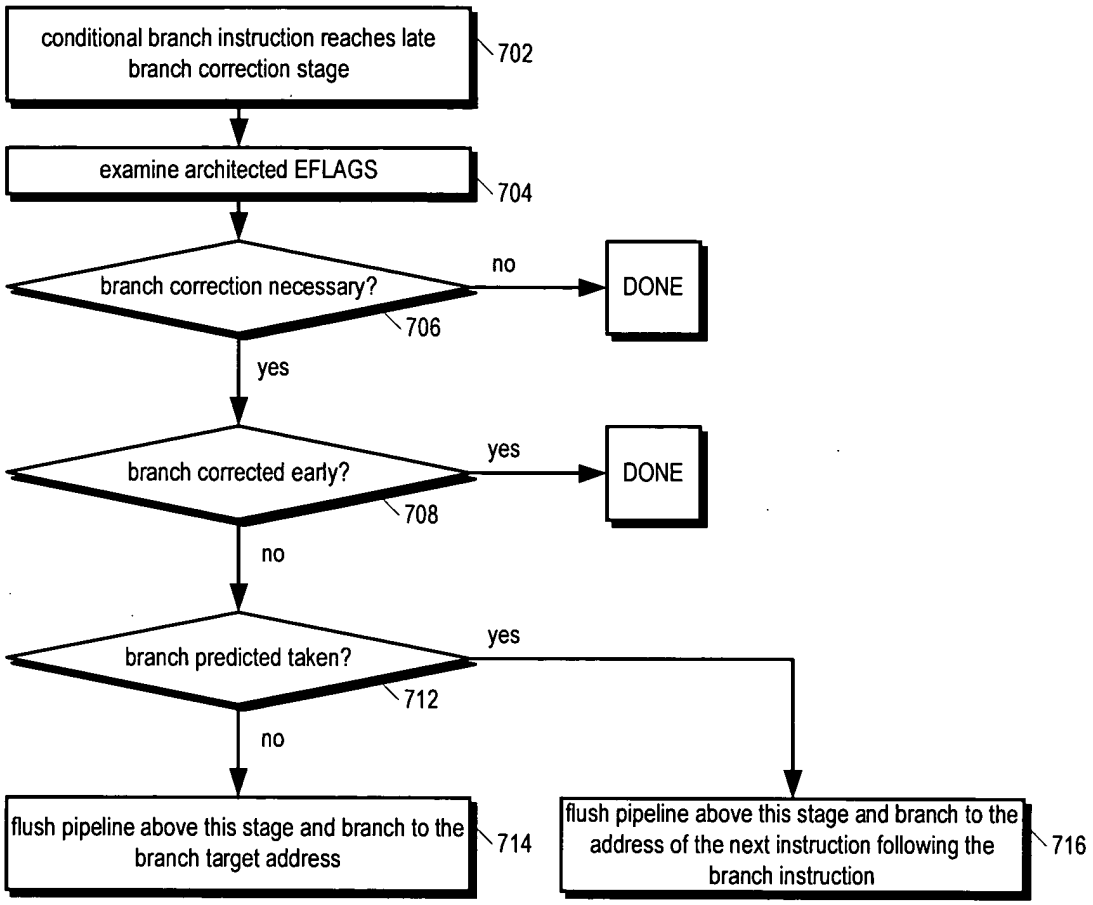


Fig. 7

Late Branch Correction